

# GA-F2A68HM-H

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APU\_VDDIO\_SUS=DDR15V  
APU\_VTT\_SUS=DDRVTT  
APU\_VDDP\_RUN=APU\_VDDR\_RUN=APU\_VDDP  
  
+1.1V\_RUN=FCH\_VDD\_11\_RUN=VCC\_SB  
  
+3.3V\_RUN=VCC3  
+3.3V\_ALW=3VDUAL

GIGABYTE™

Title

COVER SHEET

Size

Custom

Date:

Wednesday, December 17, 2014

Document Number

GA-F2A68HM-H

Rev

1.1

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25



**Model Name:GA-F2A68HM-H**


### Component value change history

**Version: 1.1**  
9MF278MS2-00  
P-Code: U13116-0

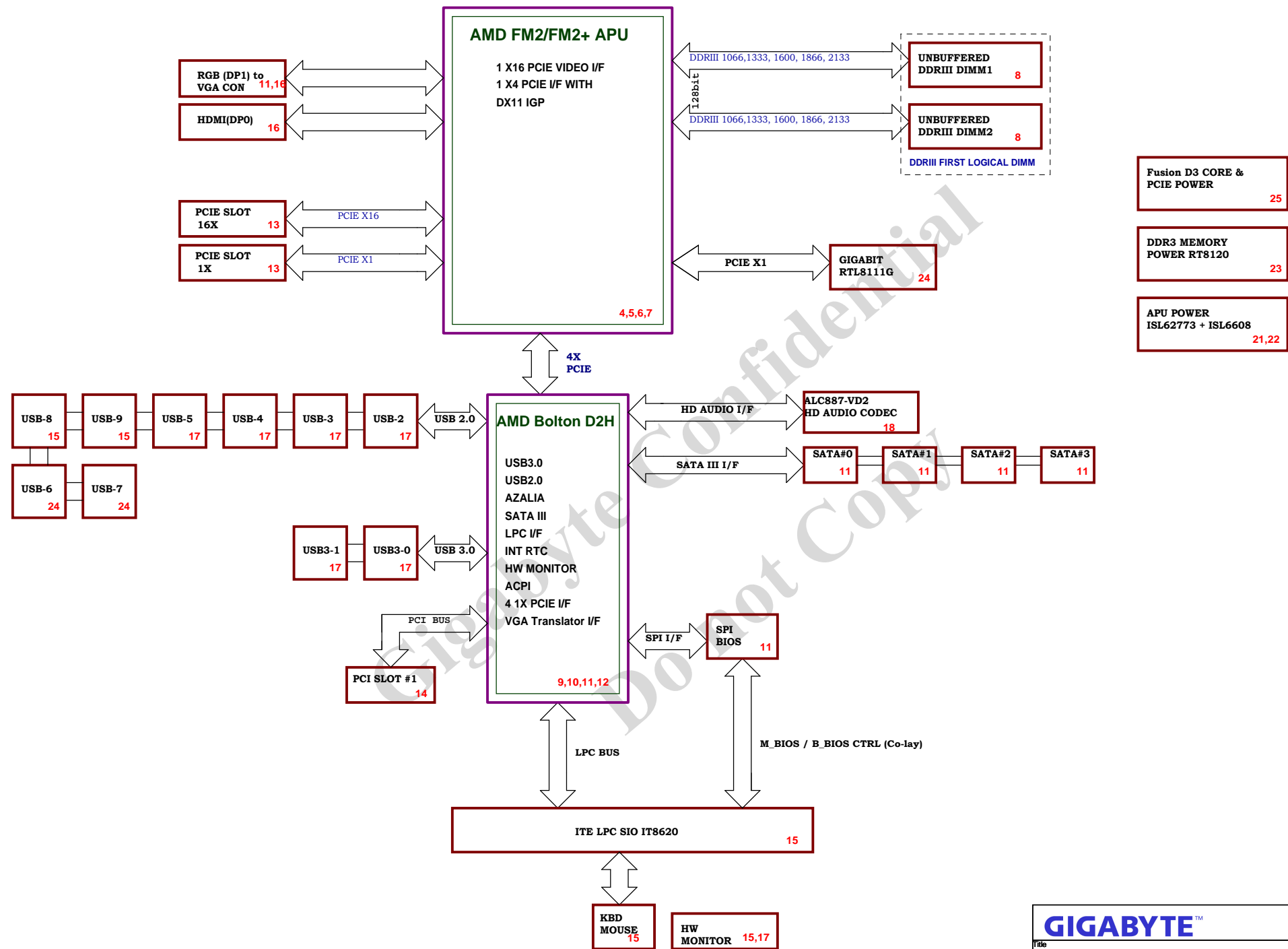
[illegible]

### Circuit or PCB layout change for next version

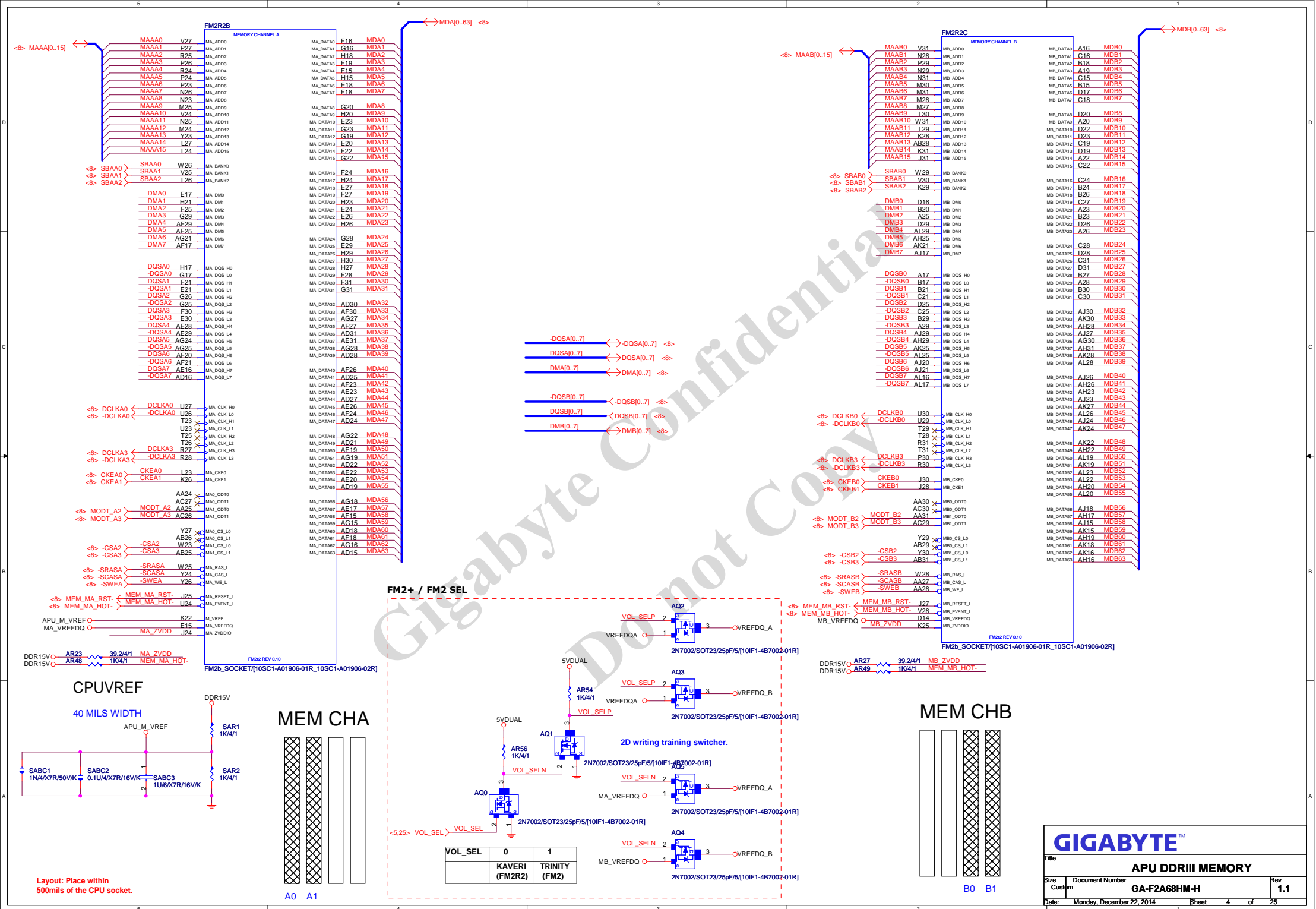
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<b>BOM &amp; PCB HISTORY</b>				
Size	Document Number			Rev
Custom	<b>GA-F2A68HM-H</b>			<b>1.1</b>
Date:	Tuesday, December 23, 2014	Sheet	2	of 25

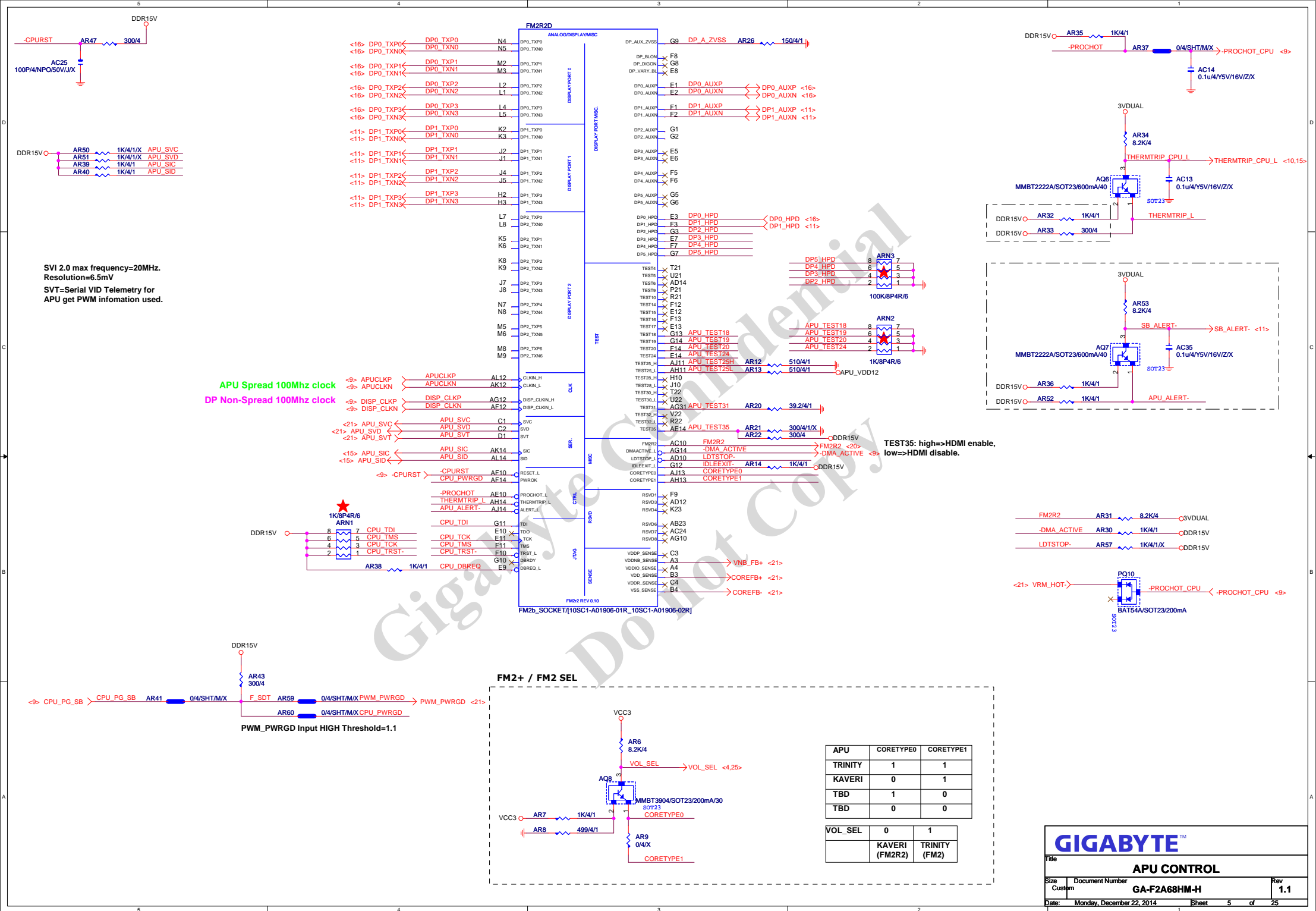




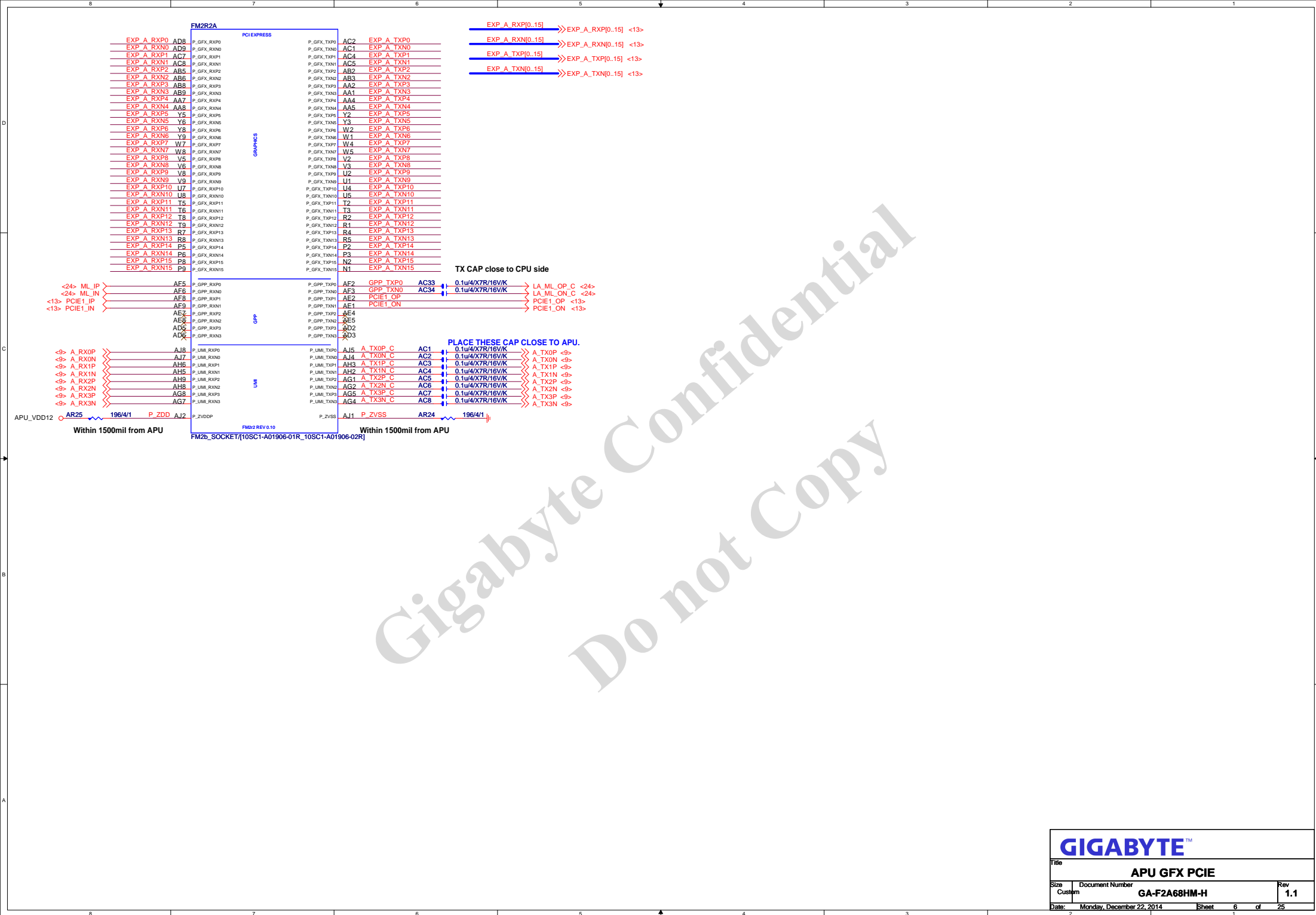




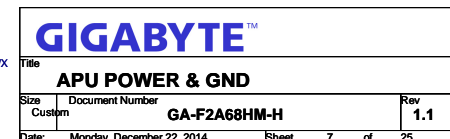
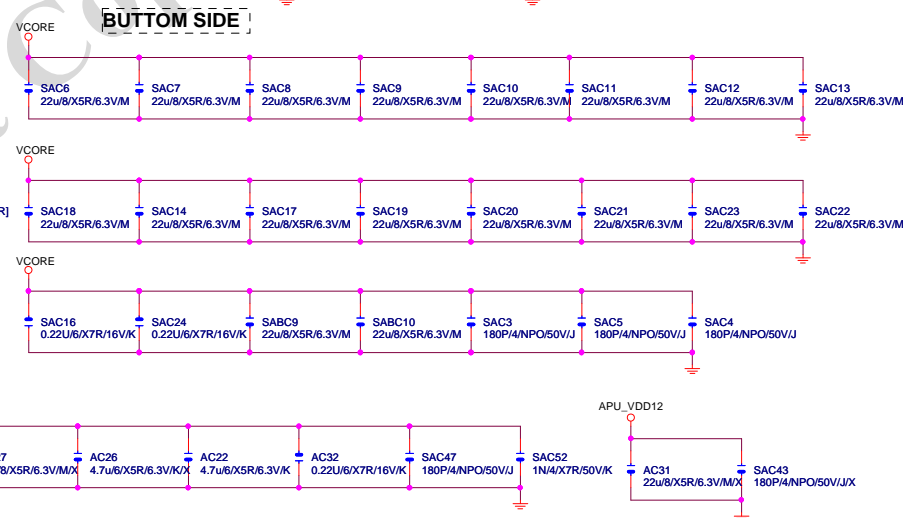
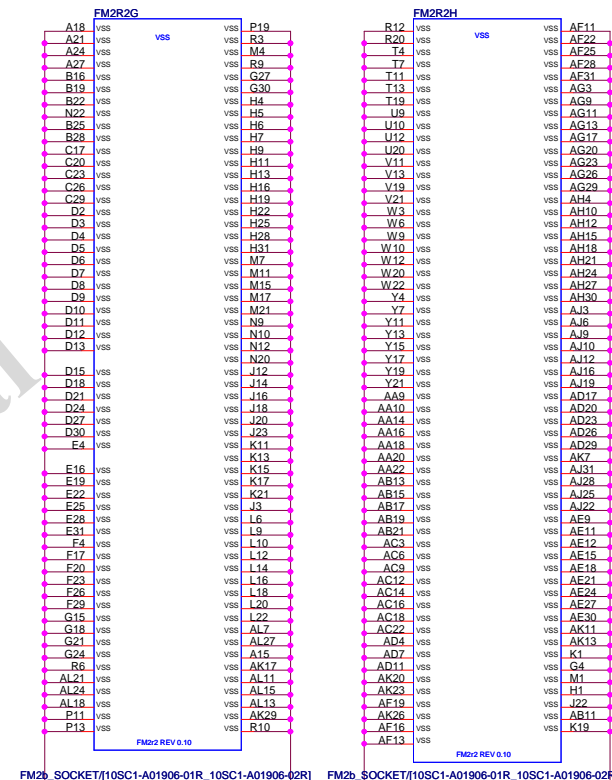
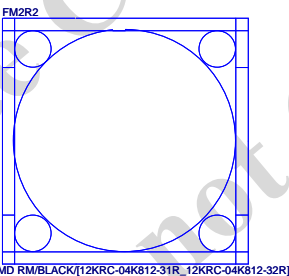
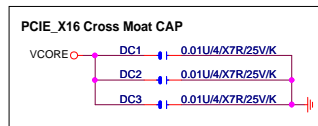




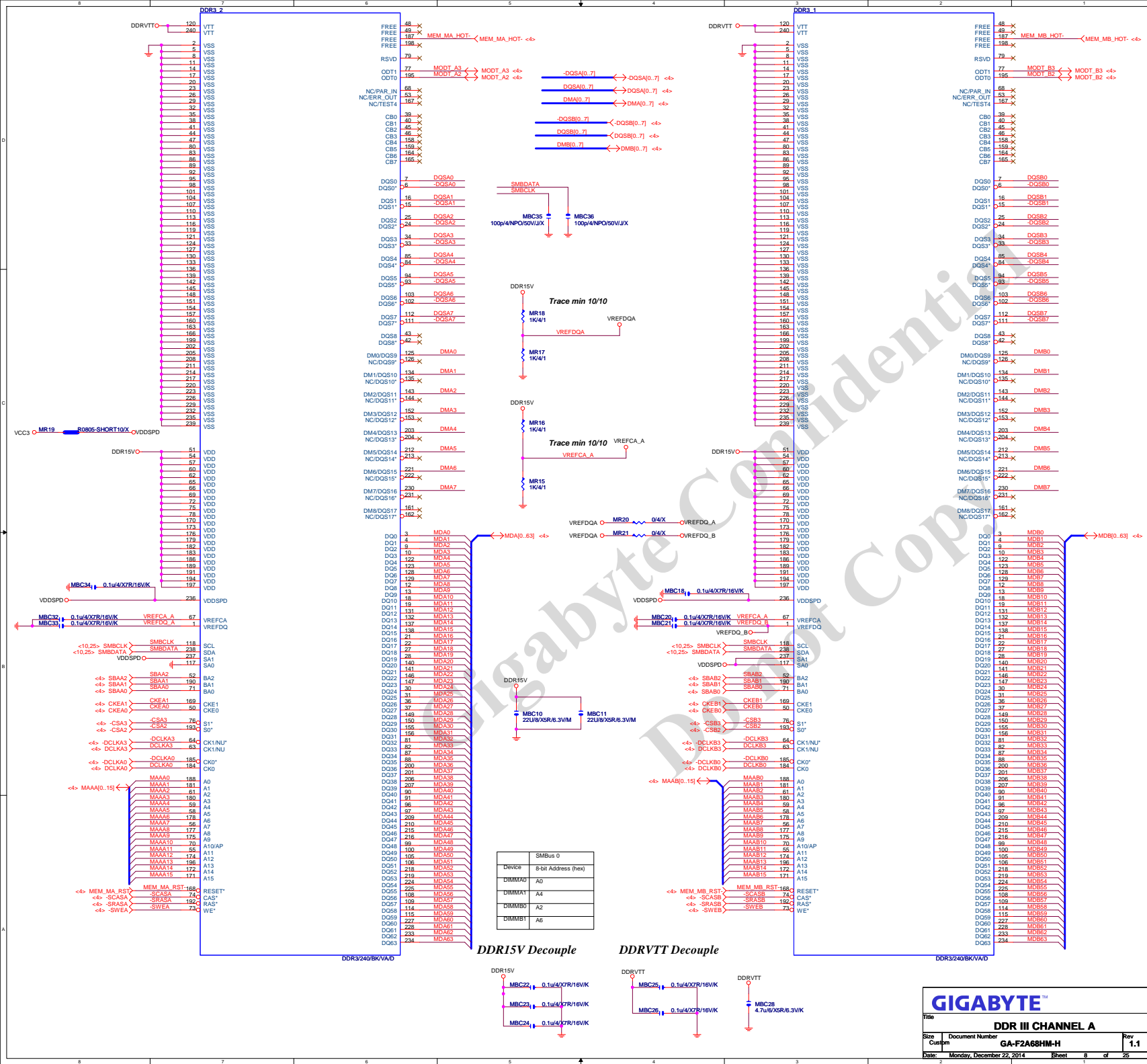










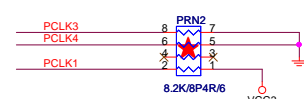
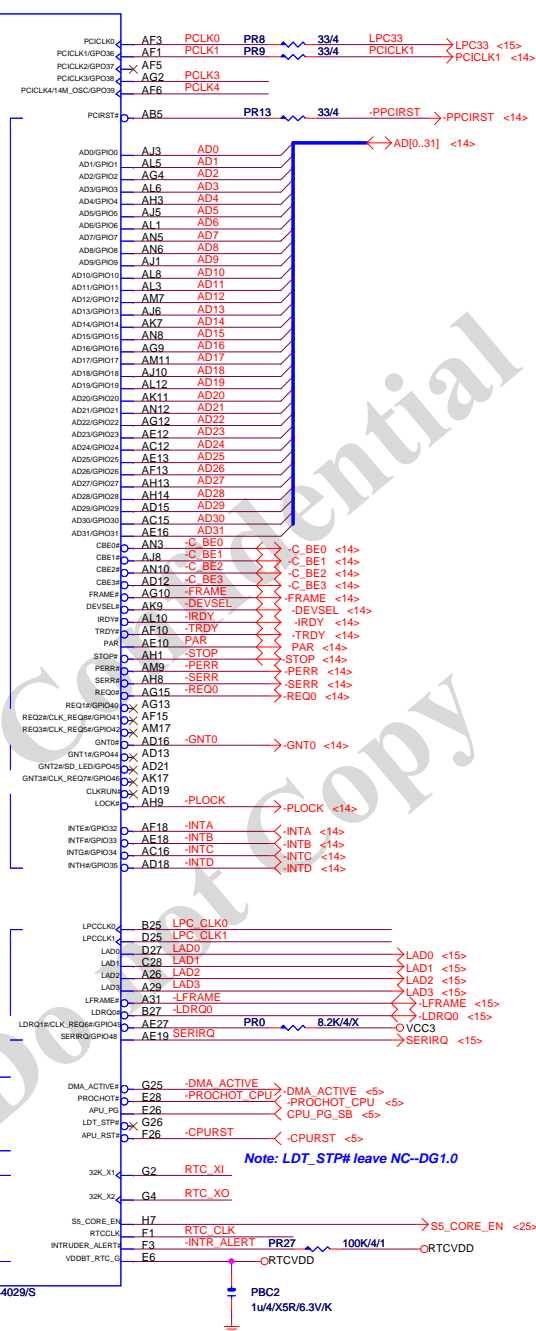
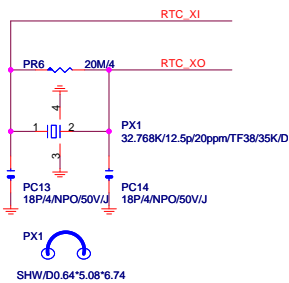






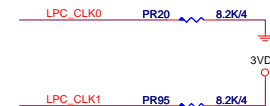
SB\_HS

SB\_HS[12SP2-SA0301-11R\_12SP2-SA0301-12R\_12SP2-SA0301-13R]

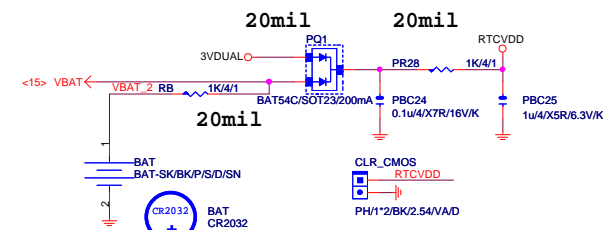


	PCLK3
PULL HIGH	USE DEBUG STRAPS
PULL LOW	IGNORE DEBUG STRAPS DEFAULT

**CLKGEN Mode:** Only for integrated clock mode.



	LPC_CLK0	LPC_CLK1
L	IMC	CLKGEN
H	ENABLED	ENABLED
	AOD Extreme	
L	IMC	CLKGEN
V	DISABLED	DISABLED
	DEFAULT	DEFAULT



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

**NOT ADD ICT FOR RTCVDD PIN**

**GIGABYTE™**

Title **Bolton D3 PCIE/PCI/CPU/LPC**

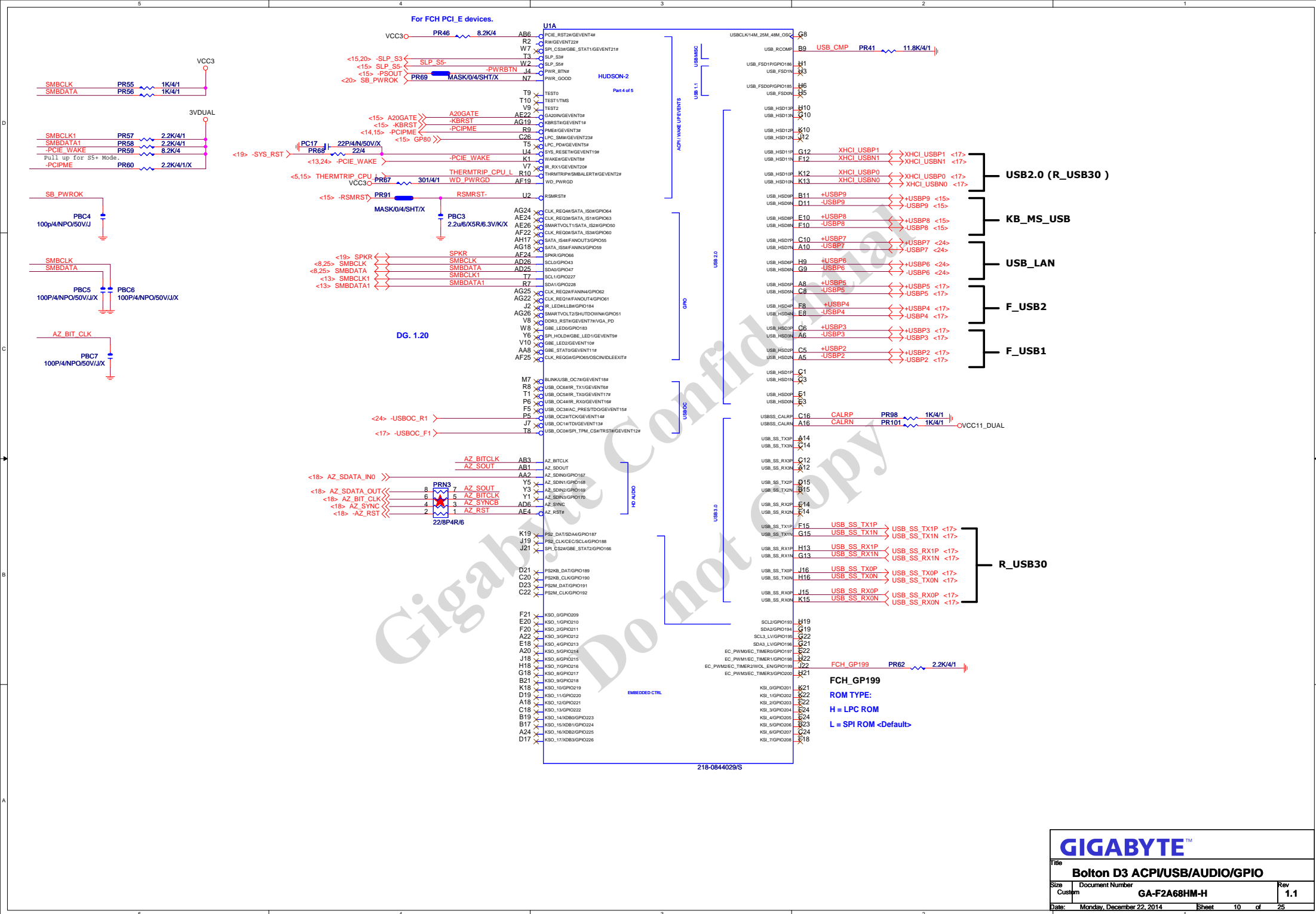
Size	Document Number
Custom	<b>GA-F2A68HM-H</b>

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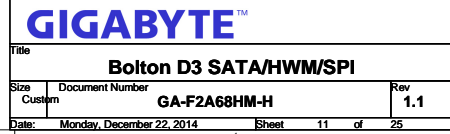
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→ S5\_CORE\_EN <25>







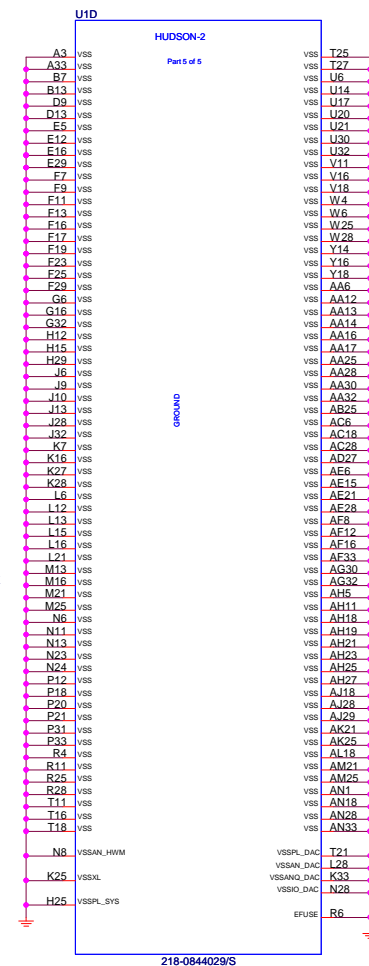
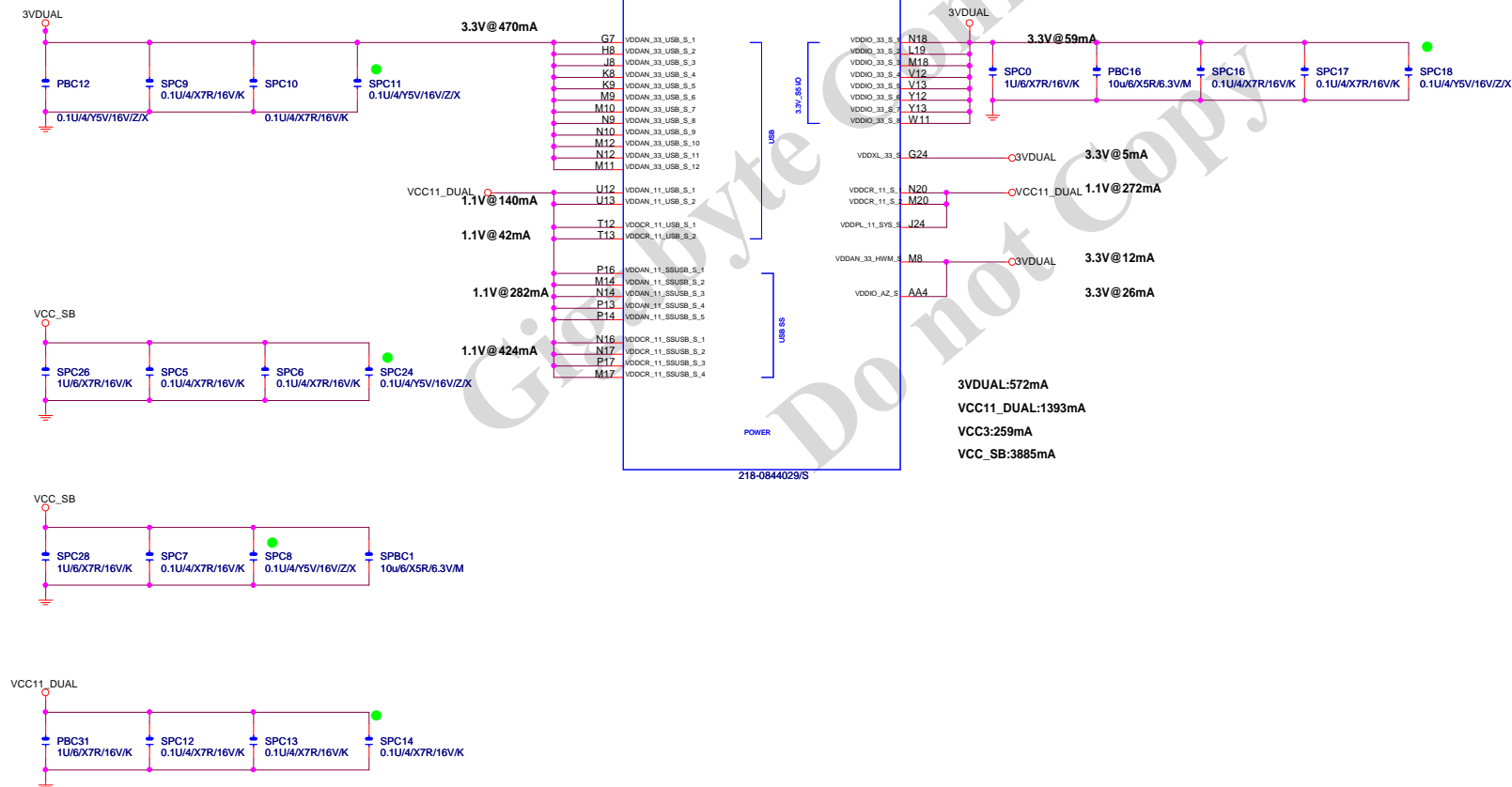




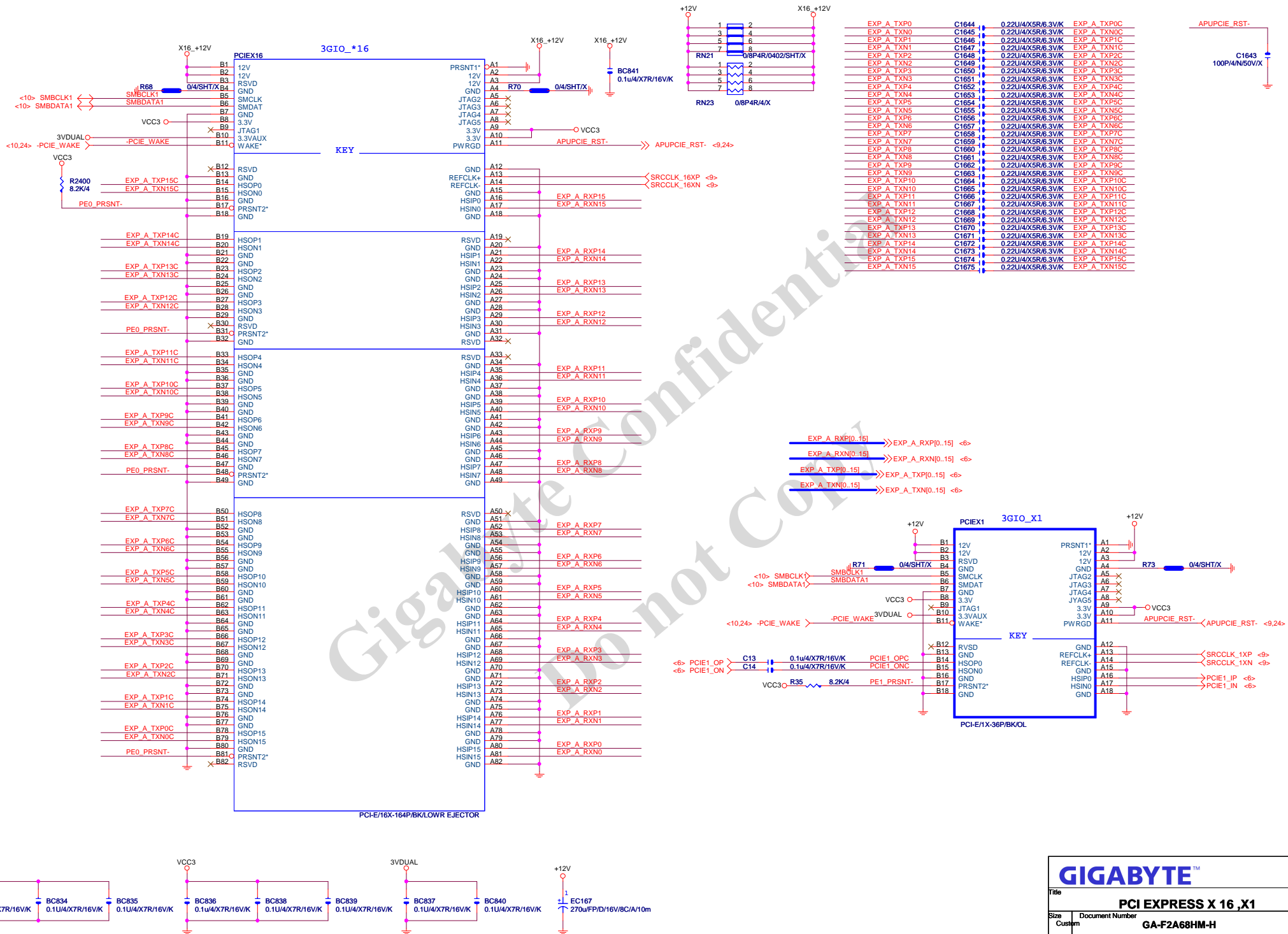


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

Hudson 3/4 does not support an RGMII/MII interface.



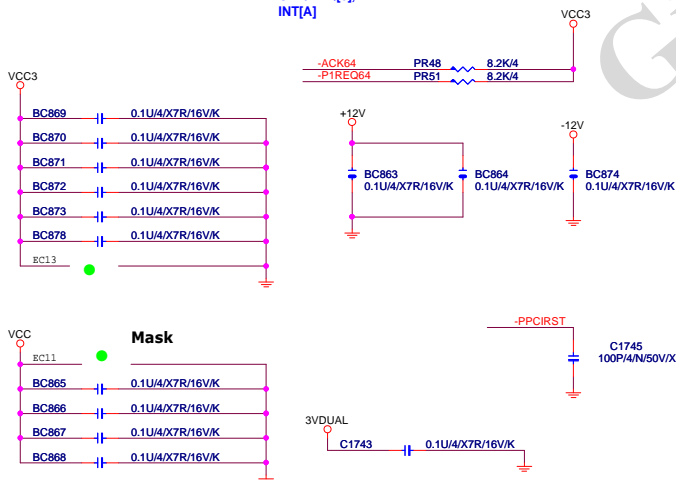
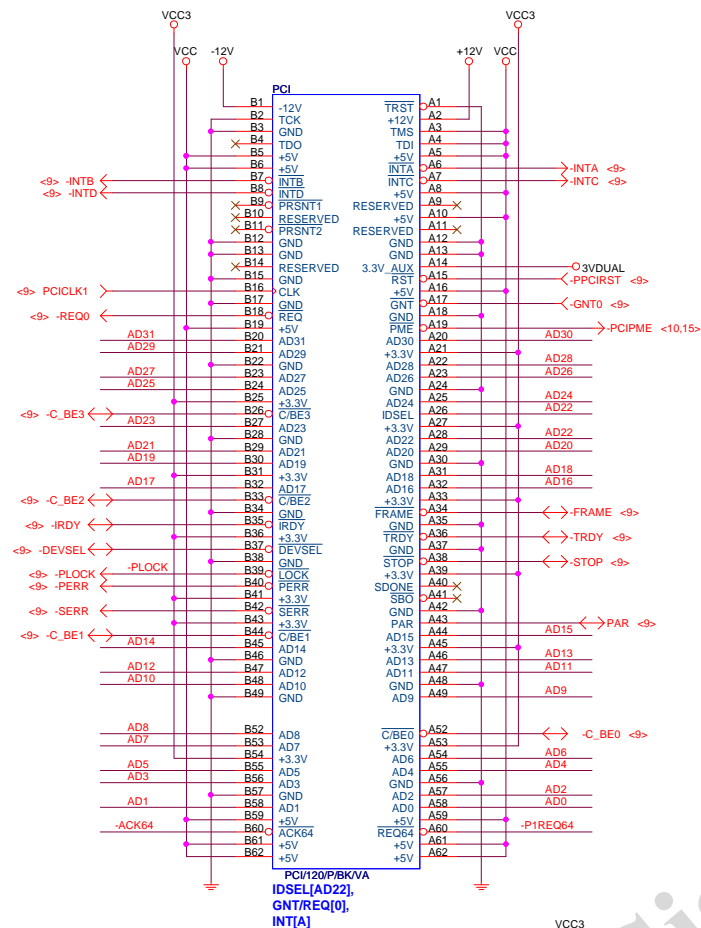






# PCI SLOT 1,2

<9> AD[0..31] <-> AD[0..31]



**GIGABYTE**

Title **PCI SLOT**

Size Custom

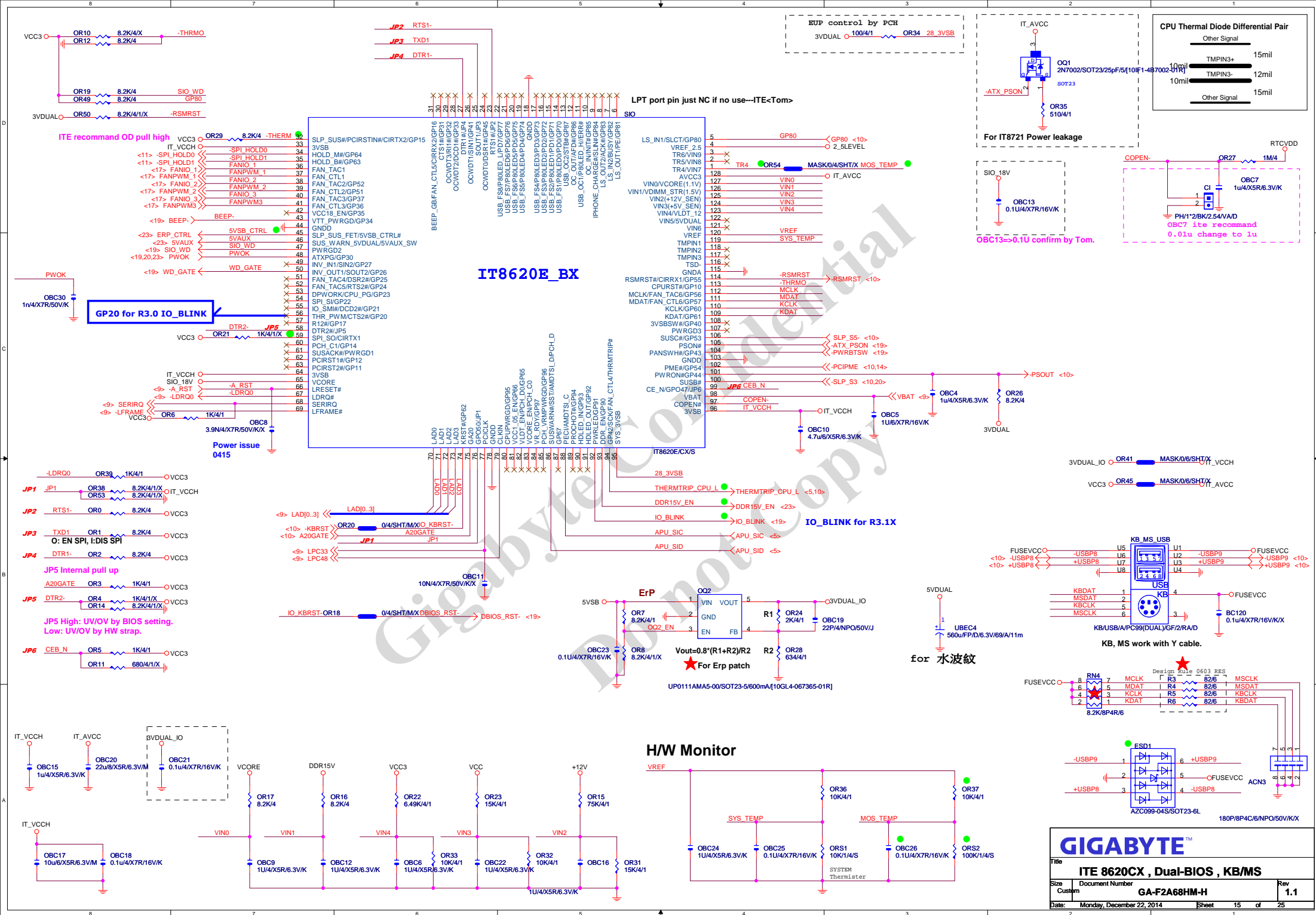
Document Number **GA-F2A68HM-H**

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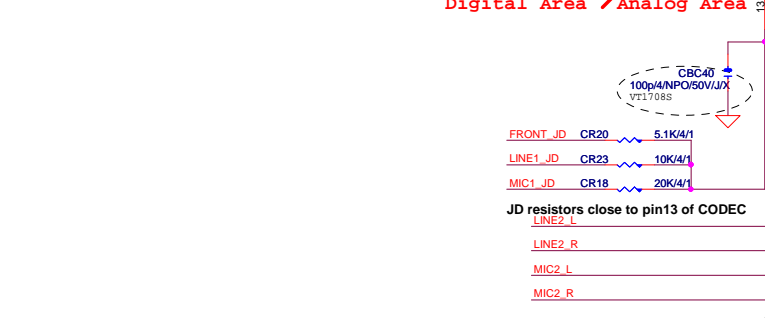
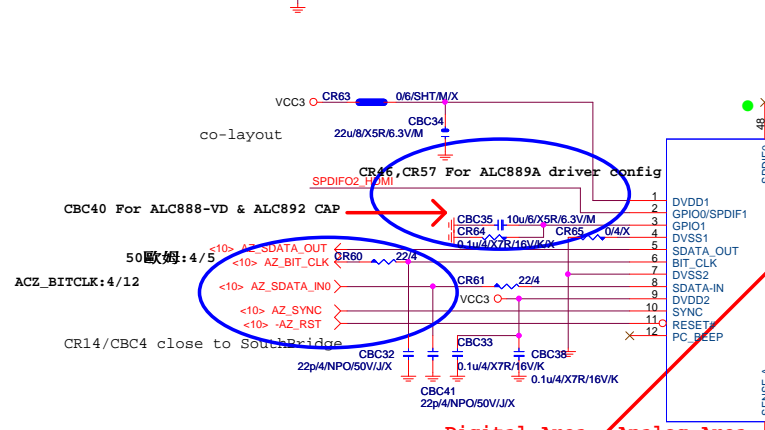
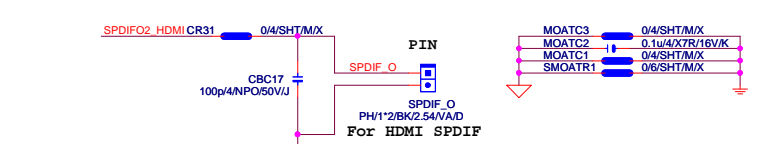








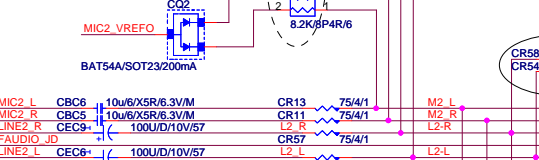
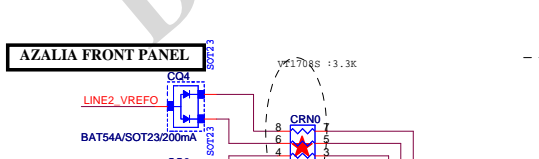
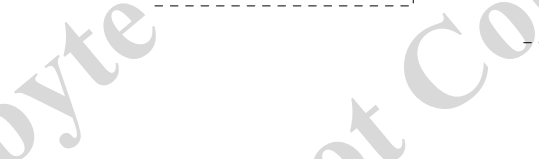
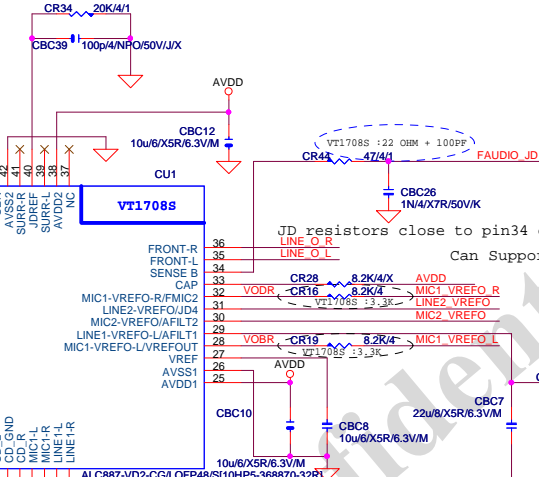
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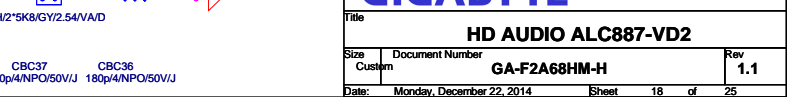
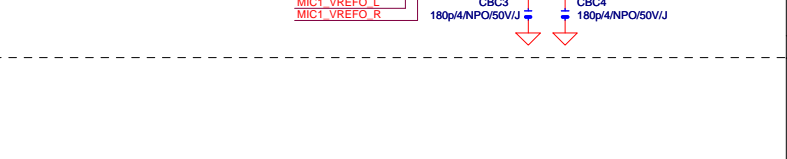
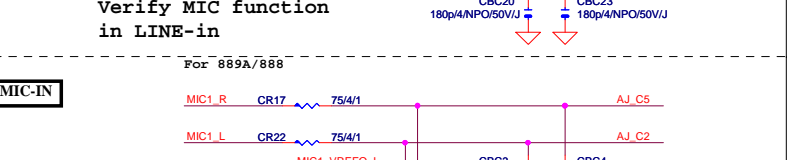
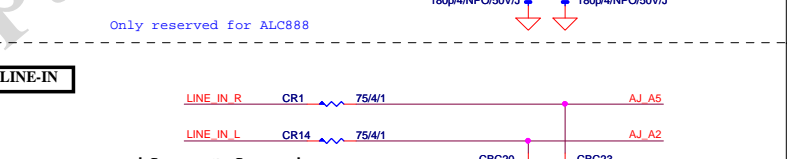
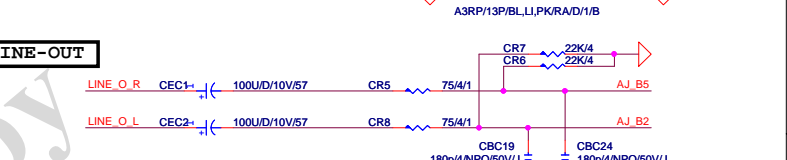
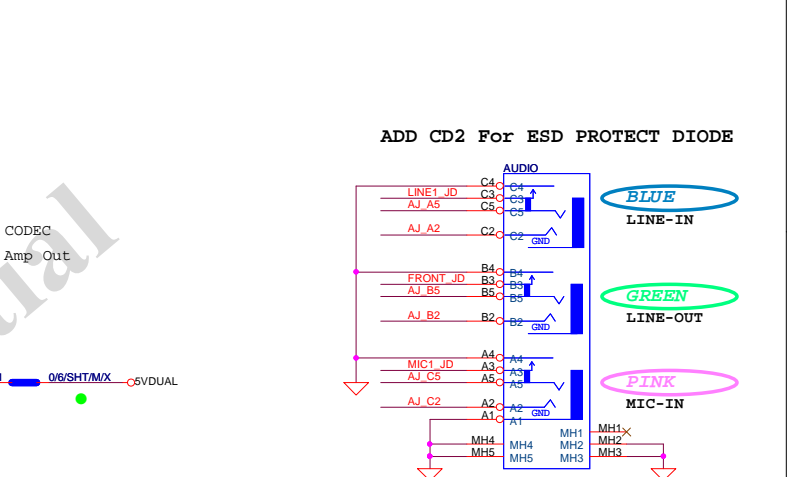
AZALIA CODEC ALC887-VD2/ALC889/VT1708S/VT1708SCE Colay

	ALC887-VD2	ALC889	VT1708S	VT1708SCE
CR65	X	O	O	X
CR64	X	X	X	O
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P
CR34	20K/1%	20K/1%	5.1K/1%	20K/1%
CR31	O	O	O	O
CR30	X	X	X	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R	22uF/X5R
CR20	5.11K/4/1	5.11K/4/1	5.1K/4/1	5.1K/4/1
CBC35	O	X	X	O
CBC39/CBC40	N/A	N/A	100P/4	100P/4
CR6/CR7/CR54/CR58	22K/4	22K/4	10K/4	10K/4
CR5/CR8/CR13/CR11/ CR57/CR53	75 ohm	62 ohm	75 ohm	75 ohm
CR51/CD1/CBC7	O	X	X	O
CD2/CD3/CQ3/CQ5	X	O	O	X
CR1/CR14/CR17/CR22	75 ohm	62 ohm	1K ohm	1K ohm

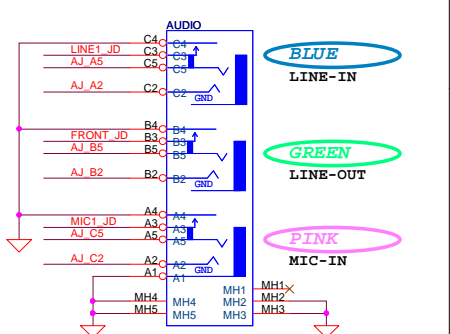
CODEC POWER/EMI PAD



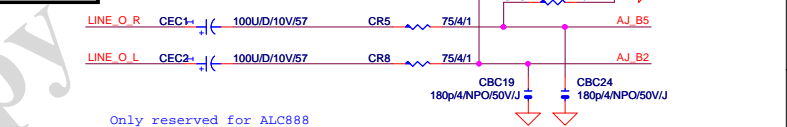
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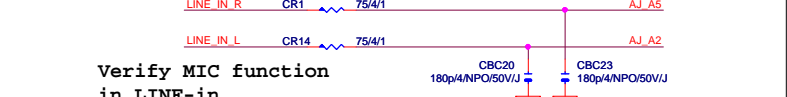
ADD CD2 For ESD PROTECT DIODE



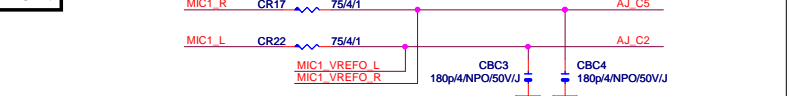
LINE-OUT



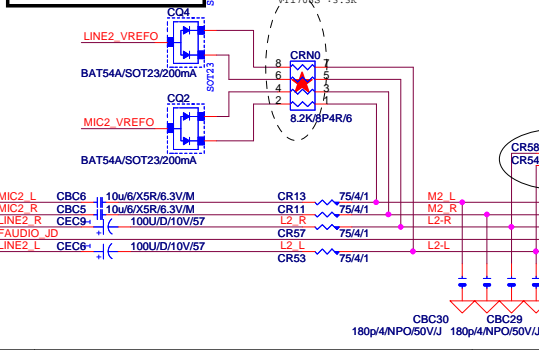
LINE-IN



MIC-IN



AZALIA FRONT PANEL



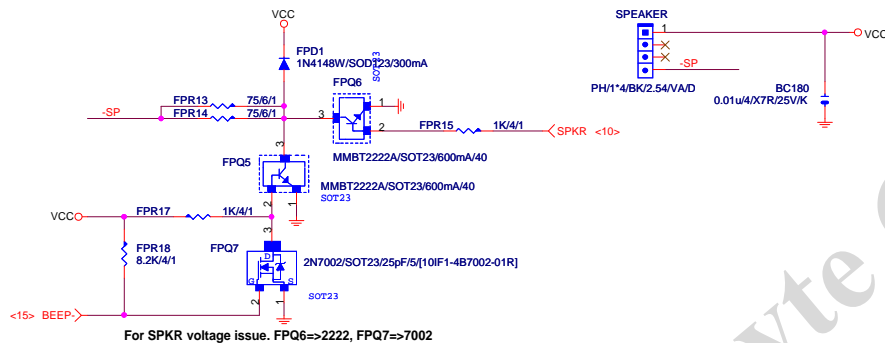
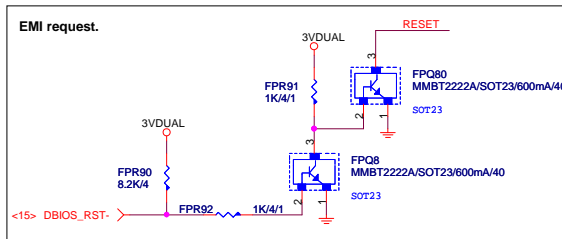
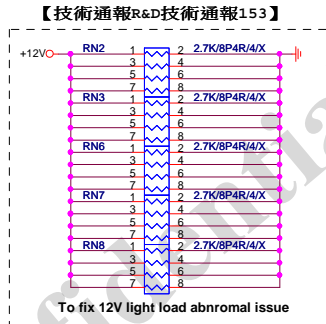
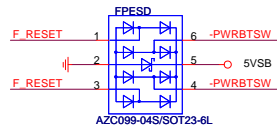
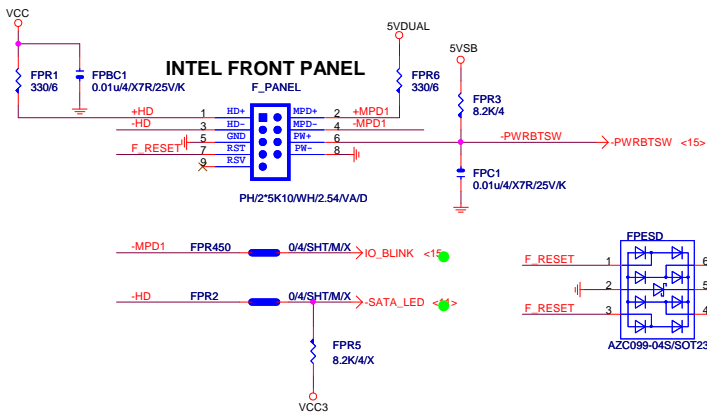
**GIGABYTE**

HD AUDIO ALC887-VD2

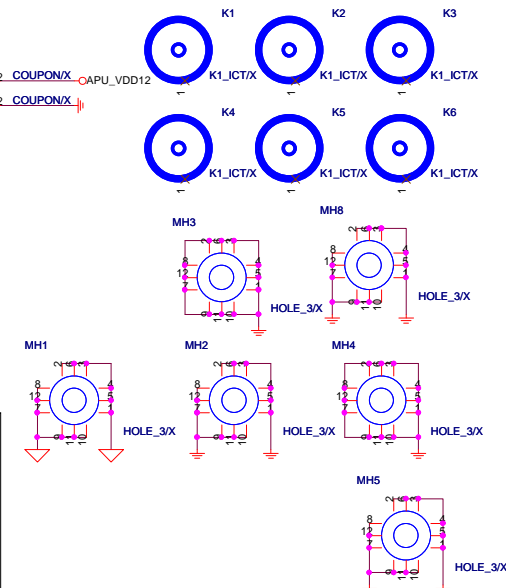
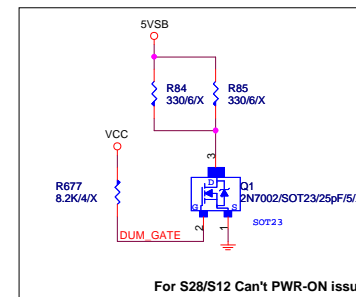
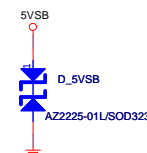
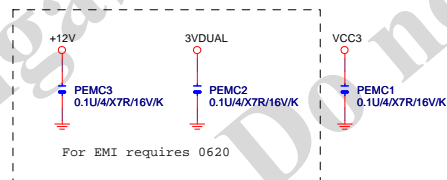
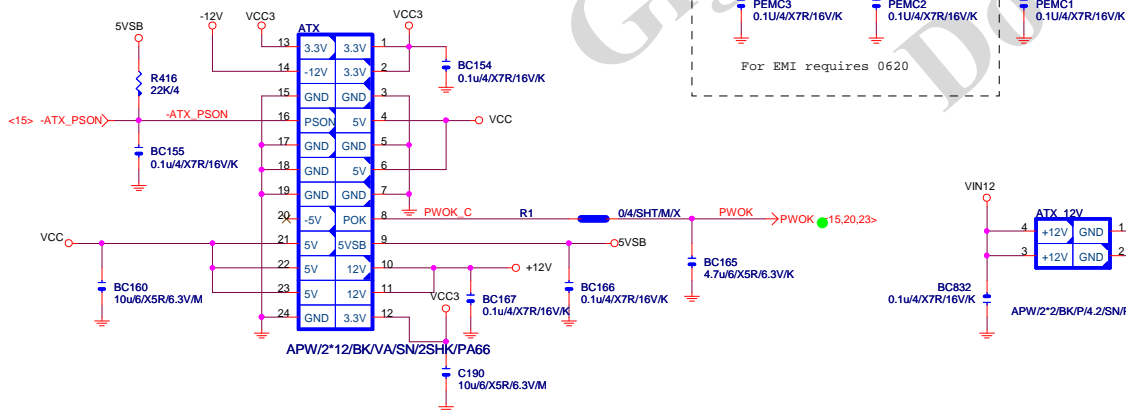
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Rev 1.1

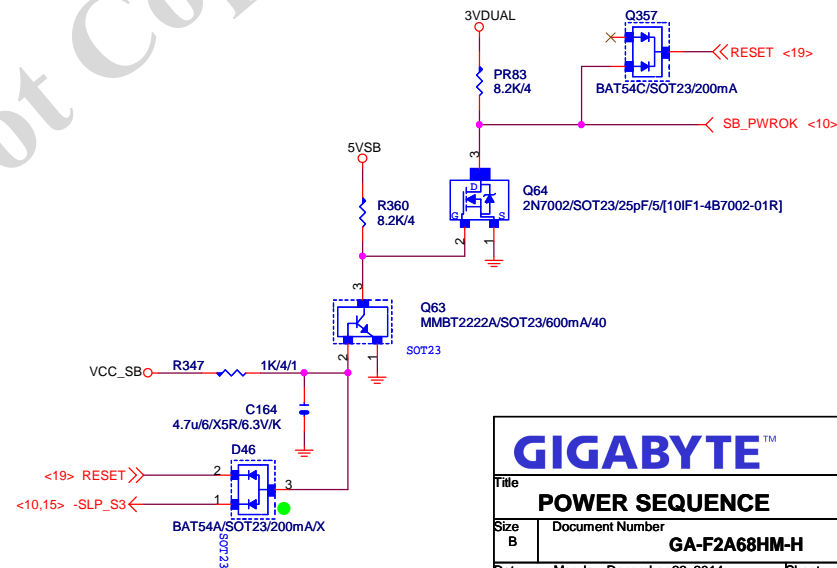
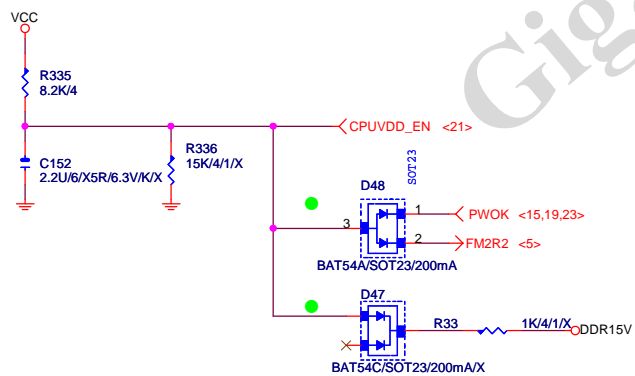
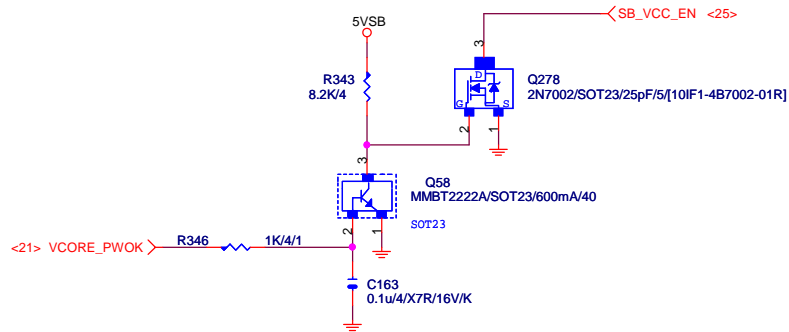




## ATX POWER CONNECTOR





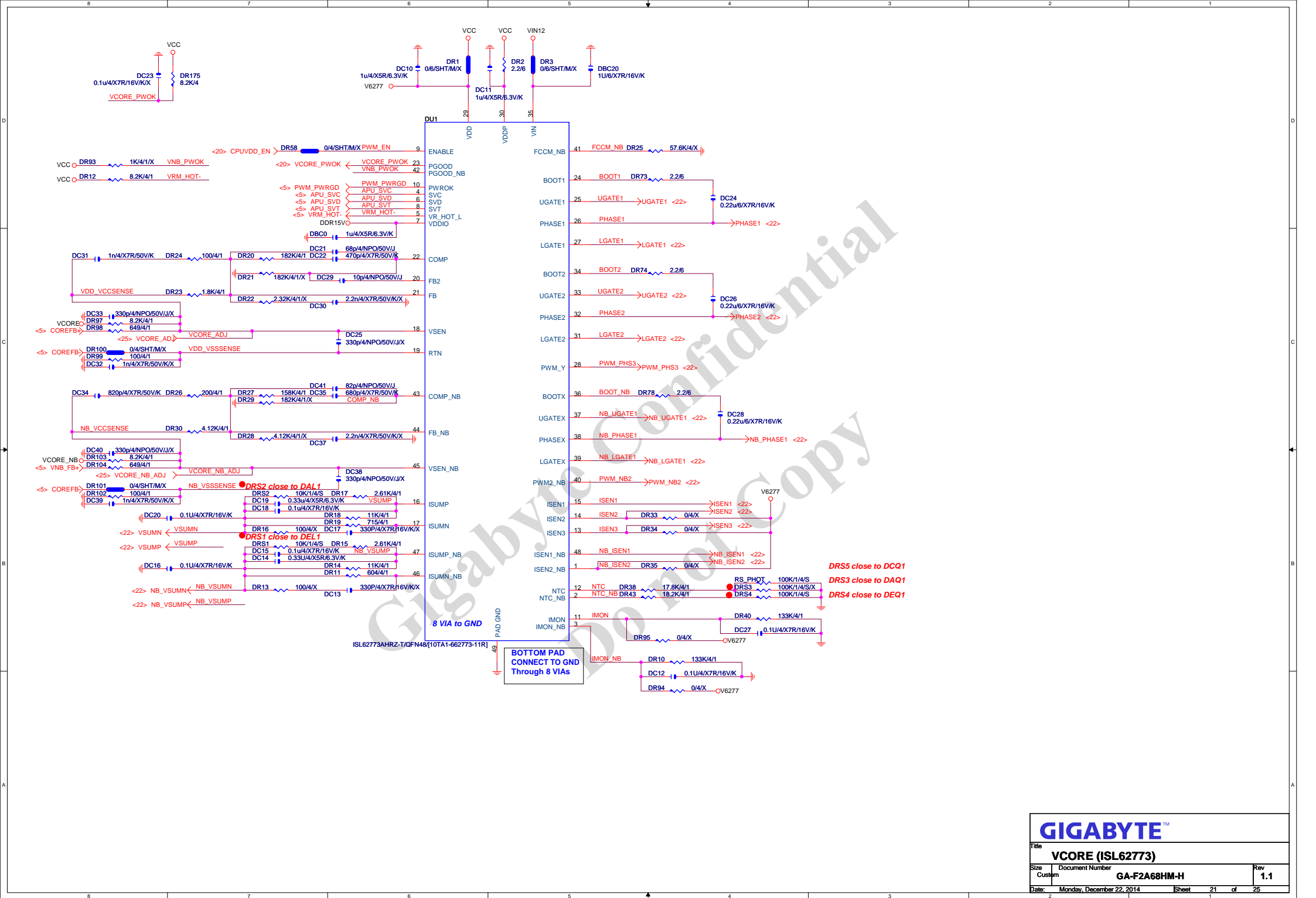


**GIGABYTE™**

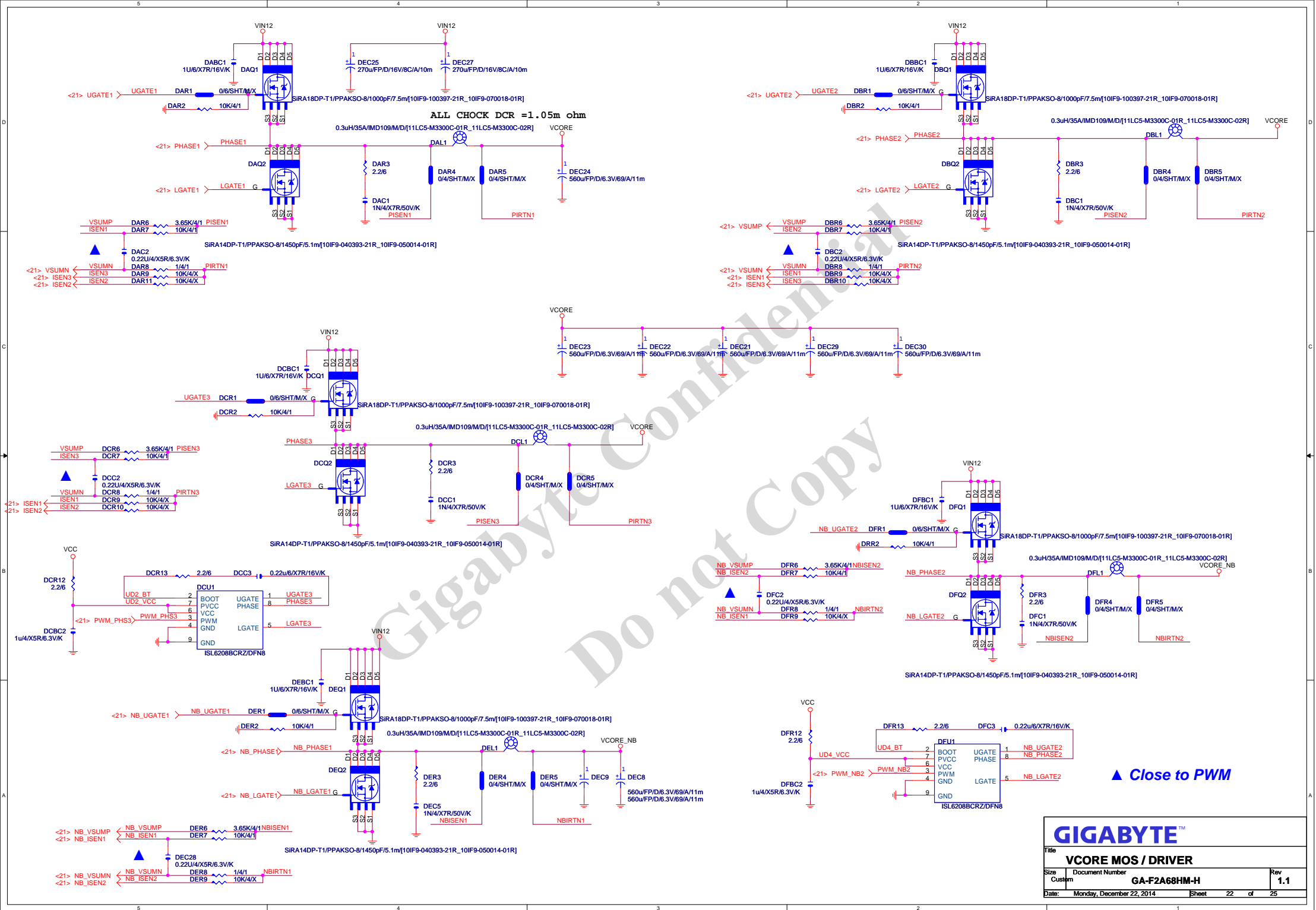
**POWER SEQUENCE**

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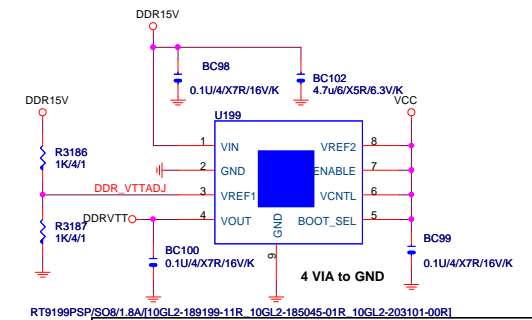
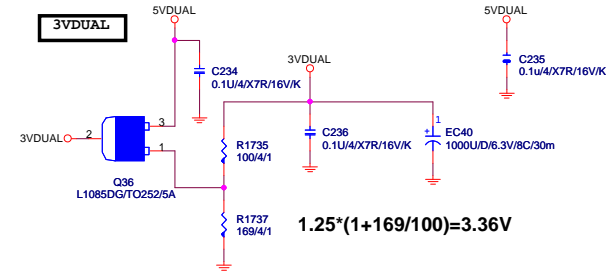






GIGABYTE™		
Title		
VCORE MOS / DRIVER		
Size	Document Number	Rev
Custom	GA-F2A68HM-H	1.1
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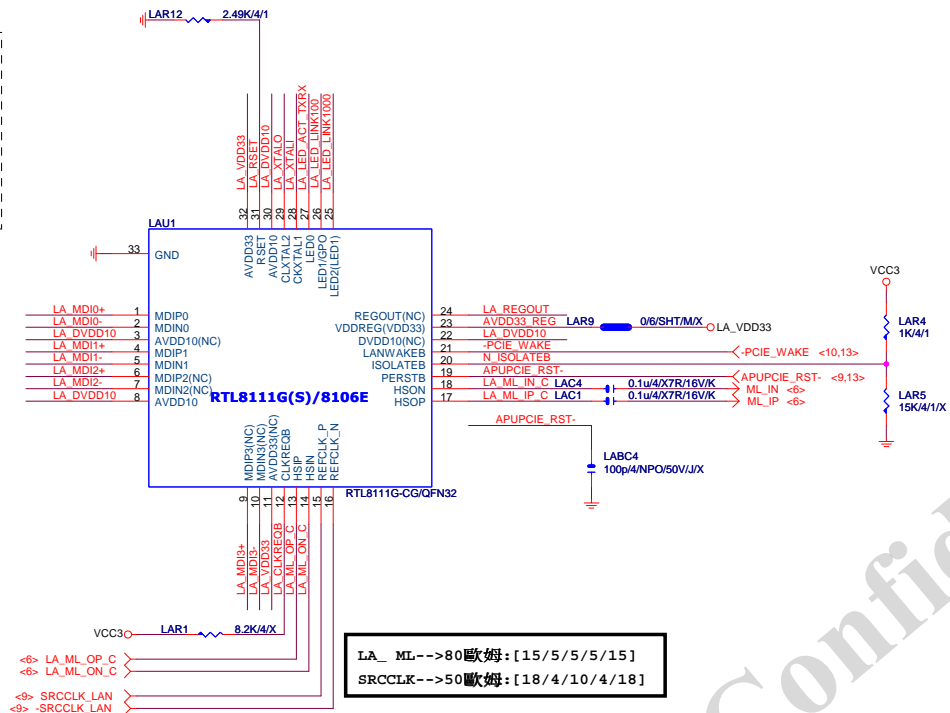
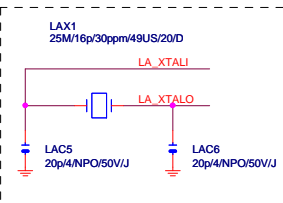




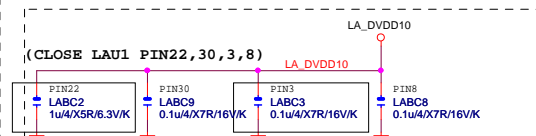
Title			
<b>DDR POWER , 5VDUAL , ErP</b>			
Size	Document Number	Rev	
Custom	<b>GA-F2A68HM-H</b>	<b>1.1</b>	
Date:	Monday, December 22, 2014	Sheet	23 of 25



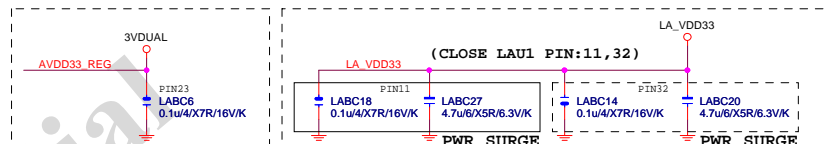
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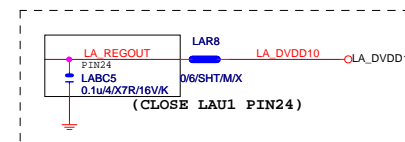
## LAN POWER



```
| LABC2:1U CLOSE PIN22[REALTEK REQ]
```

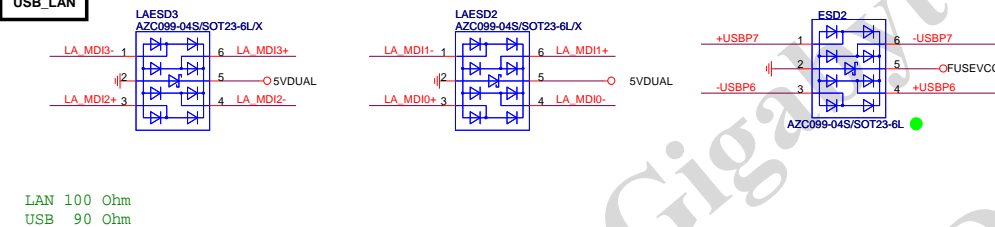


```
| LABC18,27:CLOSE PIN11[REALTEK SURGE]
| LABC14,20:CLOSE PIN32[REALTEK SURGE]
```

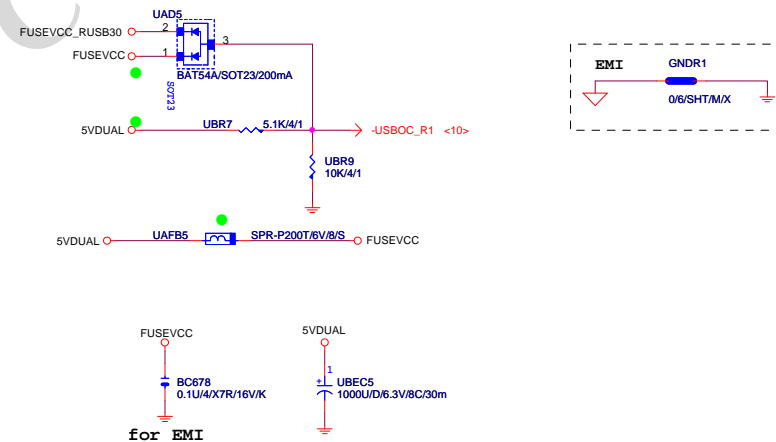
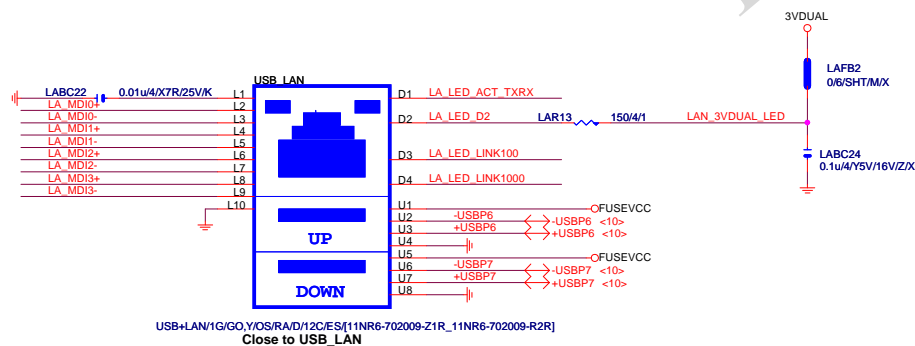


NOTE:  
RT8106E:PIN3,11,22,24-->NC  
LABC2LABC3,LABC5,LABC18,LABC27-->N/A

## USB LAN

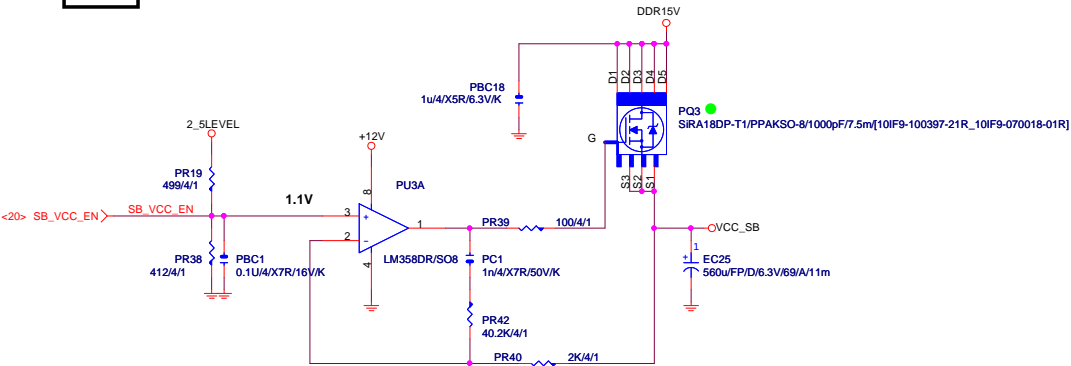


## USB\_LAN CONNECTOR



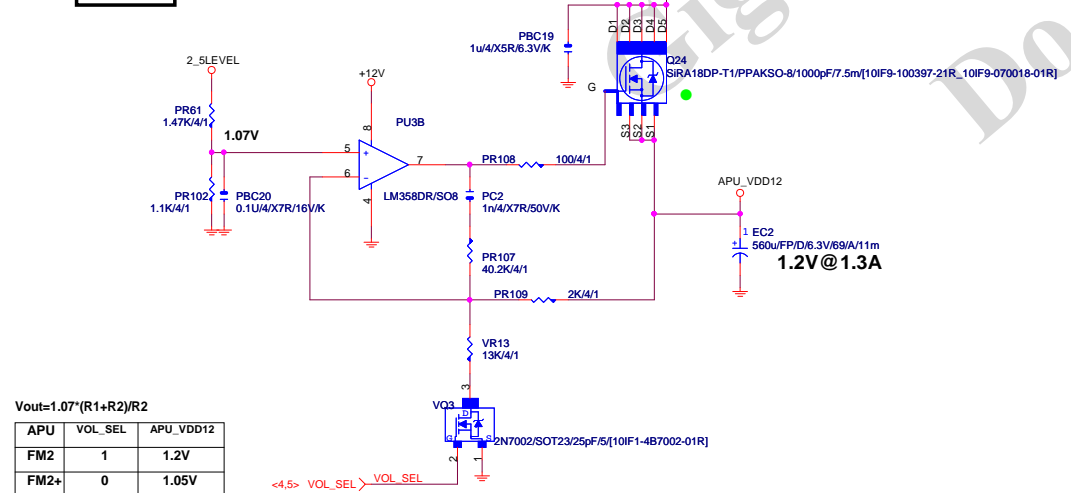


# VCC\_SB



2\_SLEVEL  
BC0  
22u/8/X5R/6.3V/M  
Near PR19 / PR61

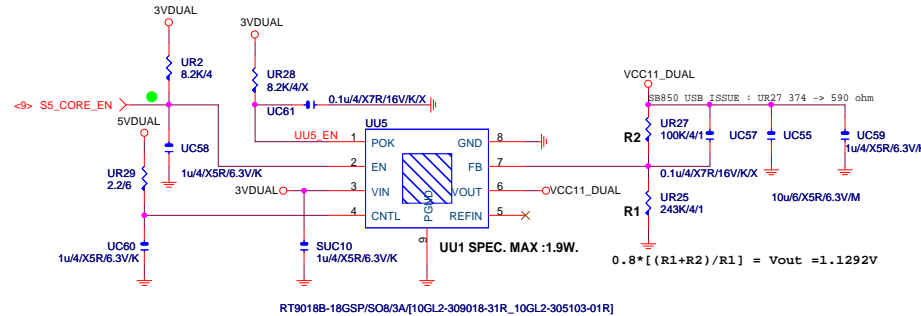
# APU\_VDDP



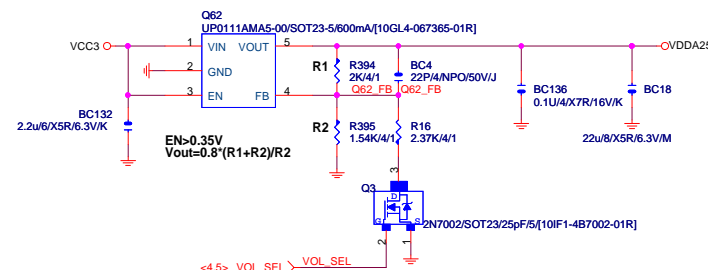
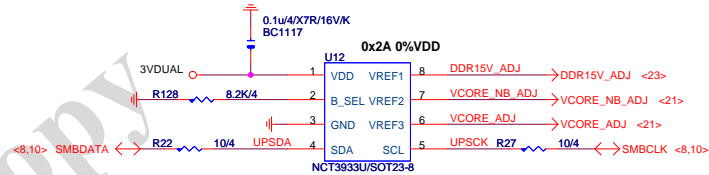
Vout=1.07\*(R1+R2)/R2

APU	VOL_SEL	APU_VDD12
FM2	1	1.2V
FM2+	0	1.05V

<4,5> VOL\_SEL < VOL\_SEL



【技術通報R&D技術通報156】  
RT9018 (RICHTEK) 與 NCT3730 (NUVOTON),  
EM5103GE (EMC) 做共用, 針對PIN7 (FB) 分壓阻值部份  
(R1/R2) 須做修改為100K以上電阻值



APU	VOL_SEL	VDDA25
FM2	1	2.5V
FM2+	0	1.8V

**GIGABYTE**

Title: **VCC\_SB, APU\_VDDP, VCC11\_DUAL, VDDA25**

Size: Custom Document Number: **GA-F2A68HM-H** Rev: **1.1**

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